

IN THE CLAIMS

Please amend claims 1, 4, 7, 8-10, and 15-17 as follows. All claims have been provided as a courtesy to the Examiner.

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1 1. (Twice Amended) A system comprising:  
2 a system memory controller; and  
3 a first memory module comprising:  
4 a first plurality of memory devices;  
5 a first memory module controller coupled to the system memory controller  
6 and the first plurality of memory devices, the first memory module controller [being  
7 configured] to receive from the system memory controller a first memory  
8 transaction in a first format and to convert the first memory transaction into a  
9 second memory transaction in a second format for the first plurality of memory  
10 devices, the second format of the second memory transaction being different from  
11 the first format of the first memory transaction.

1 2. (Unchanged) The system of claim 1, further comprising:  
2 a first memory bus coupled between the system memory controller and the first  
3 memory module controller.

1 3. (Unchanged) The system of claim 2, wherein the first memory bus comprises a  
2 signal line for a clock signal.

1 4. (Twice Amended) The system of claim 2, wherein the first memory bus  
2 comprises:  
3 a signal line for a handshake signal that indicates [when] if the first memory module  
4 controller is communicating data to the system memory controller.

1 5. (Unchanged) The system of claim 2, further comprising:  
2 a second memory bus coupled between the first memory module controller and the  
3 first plurality of memory devices.

1 6. (Unchanged) The system of claim 5, wherein the second memory bus comprises:  
2 a signal line for a clock signal.

1 7. (Twice Amended) The system of claim 5, wherein the first memory bus  
2 [operates] is to operate at a first data rate and the second memory bus [operates] is to  
3 operate at a second data rate, and wherein the first data rate is different than the second data  
4 rate.

1 8. (Twice Amended) The system of claim 5, wherein the first memory bus has a  
2 first number of signal lines and the second memory bus has a second number of signal lines,  
3 and wherein the first number of signal lines is different than the second number of signal  
4 lines.

3  
1 9. (Twice Amended) The system of claim 5, wherein the first memory module  
2 controller comprises:  
3 request handling circuitry [configured] to receive the first memory transaction from  
4 the first memory bus; and  
5 control logic coupled to the request handling circuitry and [configured] to reformat  
6 the first memory transaction into the second memory transaction on the second memory  
7 bus.

1 10. (Twice Amended) The system of claim 2, wherein the first memory bus is  
2 [configured] to carry time-multiplexed data and address information, and wherein the  
3 second memory bus includes separate address and data lines.

1 11. (Unchanged) The system of claim 1, wherein the first memory module is a dual in-  
2 line first memory module (DIMM).

1 12. (Unchanged) The system of claim 1, wherein the first memory module is a single  
2 in-line first memory module (SIMM).

1 13. (Unchanged) The system of claim 1, wherein the first plurality of memory devices  
2 comprise volatile memory devices.

1 14. (Unchanged) The system of claim 1, wherein the first plurality of memory devices  
2 comprise nonvolatile memory devices.

1 15. (Twice Amended) The system of claim 1, further comprising a second memory  
2 module including:  
3 a second plurality of memory devices;  
4 a second memory module controller coupled to the system memory controller and  
5 the second plurality of memory devices, the second memory module controller [being  
6 configured] is to receive from the system memory controller a third memory transaction in  
7 the first format and is to convert the third memory transaction into a fourth memory  
8 transaction in the second format for the second plurality of memory devices, the second  
9 format of the fourth memory transaction being different from the first format of the third  
10 memory transaction.

1 16. (Twice Amended) The system of claim 15, wherein the first plurality of memory  
2 devices are to store data in a different way than the second plurality of memory devices.

1 17. (Twice Amended) A system comprising:  
2 a system memory controller;  
3 a memory bus coupled to the system memory controller; and  
4 a memory unit including:  
5 a plurality of memory devices[;], and  
6 a memory module controller coupled to the memory bus and the plurality of  
7 memory devices, the memory module controller [being configured] is to receive a first  
8 memory transaction from the memory bus in a first format and is to convert the first

9 memory transaction into a second memory transaction in a second format to at least one of  
10 the plurality of memory devices, the second format of the second memory transaction being  
11 different from the first format of the first memory transaction.

1 18. (Unchanged) A method of communicating a memory transaction between a system  
2 memory controller and at least one of a plurality of memory devices on a memory module  
3 including a memory module controller, the method comprising:  
4 sending a first memory transaction from the system memory controller to the  
5 memory module controller, the first memory transaction having a first format;  
6 reformatting the first memory transaction into a second memory transaction for at  
7 least one of the memory devices, the second memory transaction having a second format  
8 that is different from the first format; and  
9 sending the second memory transaction to the at least one of the memory devices.

1 19. (Unchanged) The method of claim 18, wherein the memory transaction is a read  
2 transaction.

1 20. (Unchanged) The method of claim 18, wherein the memory transaction is a write  
2 transaction.